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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,491	03/01/2004	Brian Moore	11157-073	7561

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EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/788,491	MOORE, BRIAN
	Examiner	Art Unit
	Jimmy Nguyen	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34 - 47, 50, 54 - 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34 - 47,50, 54- 57* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

1. The amendment filed 12/19/05 has been carefully considered with the following effect;

The examiner acknowledges the terminal disclaimer filed 12/19/05.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 34 – 36, 44, 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Frey et al (US 6, 430,720).

As to claim 34, Frey et al disclose (fig 1) a test circuit (1) for testing an integrated circuit (2) on a wafer the test circuit formed on the wafer with the integrate circuit, the test circuit comprising:

A variable ring oscillator circuit including

i) a base ring oscillator circuit (18, which includes the delay circuit 70 or 50 in figs 3 – 5, column 12 lines 62 - 65)

ii) a plurality of sub-circuits (2 - 6) couple to the base ring oscillator circuit (18); and

iii) a plurality of switching elements (8, 10) for selectively coupling at least one of the plurality of sub-circuits (2 – 6) to the base ring oscillator circuit (18) ; and

iii) a control circuit (20) to selectively couple the sub-circuits (2 - 6) to the base ring oscillator circuit (18) to produce different versions of the variable ring oscillator (18) circuit associated with a selected sub-circuit,

the test circuit (1) conducts a separate test of the integrate circuit (2) for at least one of the versions of the variable ring oscillator circuit (18)

As to claim 35, Frey et al disclose (fig 1) the test circuit of claim 34 wherein each test conducted by the test circuit is a parametric test (functional test, see the abstract).

As to claim 36, Frey et al disclose (fig 1) wherein the sub circuit (2 - 6) when couple to the base ring oscillator circuit (18) change the frequency of oscillation of the variable ring oscillator circuit.

As to claim 44, Frey et al disclose (fig 1) the control circuit (20, 3) comprises a sequencer (3) to selectively couple the sub-circuits (2 - 6) to the variable ring oscillator circuit (18) to produce a series of test states.

As to claim 47, Frey et al disclose (fig 1) the test circuit produces a test result signal that is the output of the variable ring oscillator circuit (18).

As to claim 50, Frey et al disclose (fig 1) the control circuit further comprises a second ring oscillator adapted to provide a first clock signal, and a divider (24) coupled to the ring oscillator and the sequencer (3) and adapted to provide a second clock signal (TCK), wherein the second clock signal (TCK) is provided to the sequencer (3) so that the sequencer (3) can provide a series of test state signals to the variable ring oscillator circuit (18) and plurality of sub-circuits (2 –6).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 37, 38, 40, 41, 45, 46, 54 – 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al (US 6, 430,720) in view of Merrill et al (US 5,039,602).

As to claims 37, **38**, **40**, **41**, Frey et al disclosed everything except for the capacitive load. On the other hand, Merril et al disclose (fig 2) the test circuit of claim

36 wherein at least one sub- circuit comprises a capacitive load (24) to change the frequency of oscillation of the variable ring oscillator circuit.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and use the capacitive load as taught by Merrill et al for the purpose of alter the frequency of the test circuit.

As to claim 45, Frey et al disclosed everything except for the test circuit form on the wafer. On the other hand, Merril et al teachthe test circuit (22) is formed on the wafer (84) with at least tow metallization layers of the IC (86).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and use test circuit formed within the wafer for the purpose self testing.

As to claim 46, Frey et al disclosed everything except for different layers. On the other hand, Merril et al disclose (fig 2) the test circuit (22) is formed on the wafer (84) with at least one metallization layers of the IC (86) and one polysilicon layer of the IC (86).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and use test circuit formed within the wafer for the purpose self testing.

As to claims 54, **55**, Frey et al disclosed everything except for the test circuit is formed adjacent to a die. On the other hand, Merril et al disclose (fig 2) the test circuit (22) is formed adjacent to a die containing the IC (86) and on the IC (86).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and use test circuit formed within the wafer for the purpose self testing.

As to claims 56, **57,** Frey et al disclosed everything except for the test circuit is formed on a large percentage of dies on the wafer and near the edge of the wafer.

On the other hand, Merril et al disclose (fig 2) the test circuit (22) is formed adjacent to a die containing the IC (86) and on the IC (86).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and use test circuit formed within the wafer for the purpose self testing.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 39, 42, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al (US 6,430,720) in view of Merrill et al (US 5,039,602) and further in view of Lee (US 5,686,855).

As to claim 39, Frey et al disclose (fig 1) and Merril et al disclose (fig 2) disclose everything except for the sub- circuit comprises a delay element to change the frequency of oscillation of the variable ring oscillator circuit.

On the other hand, Lee teaches the sub- circuit comprises a delay element (24, 28) to change the frequency of oscillation of the variable ring oscillator circuit.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Frey et al and Merrill et al with a delay circuit of Lee for the purpose of alternate the frequency of the signal during the testing process.

As to claims 42, 43, Lee disclose the delay element (24, 28) comprises at least one inverter is CMOS inverter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571-272-1965. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramtez Nestor, can be reached on 571272 -2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN.
March 2, 2006

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
03/02/06